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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/748,098	12/21/2000	Nicholas J. Kelsey	20880-05093; Case 5093	4360
758	7590	10/19/2004		
FENWICK & WEST LLP SILICON VALLEY CENTER 801 CALIFORNIA STREET MOUNTAIN VIEW, CA 94041			EXAMINER HARKNESS, CHARLES A	
			ART UNIT 2183	PAPER NUMBER

DATE MAILED: 10/19/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

## Office Action Summary

Application No.

09/748,098

Applicant(s)

KELSEY ET AL.

Examiner

Charles A Harkness

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

### Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

### Status

- 1) ☒ Responsive to communication(s) filed on 22 July 2004.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

### Disposition of Claims

- 4) ☒ Claim(s) 1-28 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-28 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

### Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

### Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some \* c) ☐ None of:
- ☐ Certified copies of the priority documents have been received.
  - ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
  - ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

### Attachment(s)

- |  |   |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892)                        | 4) <input type="checkbox"/> Interview Summary (PTO-413)                     |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)               | Paper No(s)/Mail Date. _____  |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| Paper No(s)/Mail Date <u>8/11/04; 7/22/04</u> .  | 6) <input type="checkbox"/> Other: _____                                    |

## DETAILED ACTION

### *Claim Rejections - 35 USC § 102*

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

1. Claims 1-3, 13-17, 19 and 21-24 are rejected under 35 U.S.C. 102(e) as being anticipated by Joy et al, U.S. Patent Number 6,542,991 (herein referred to as Joy).

2. Referring to claim 1 Joy has taught a computer based system for switching between program contexts comprising:

An embedded pipelined processor (Joy figure 3, column 8 lines 14-67) capable having a first program thread and a second program thread in an execution pipeline having a thread selection hardware (Joy figure 6, column 13 lines 5-23, column 15 lines 4-7);

A first set of data storage devices capable of storing a first thread state of said embedded processor (Joy figure 5 number 510 column 13 lines 5-23);

A second set of data storage devices capable of storing a second thread state of said embedded processor (Joy figure 5 number 512 column 13 lines 5-23); and

A hardware thread scheduler for identifying which of said program threads said embedded processor executes (Joy figure 6 column 15 lines 4-7) and configurable to allocate available processing time of the embedded pipelined processor among at least the first and

second states according to a fixed schedule (Joy figure 6, column 2 lines 40-45; the priority of the scheduler would be fixed, thus giving it a fixed schedule, since it would operate the same way each time it encounters the same threads);

Wherein said thread selection hardware in the embedded pipelined processor switches between said first and second thread state after the end of the execution of a first program instruction in the first thread and before the beginning of the execution of a second program instruction (Joy column 3 lines 45-56, column 6 lines 15-35; the thread that is idle would have completed a thread, and the second thread would not be able to execute a thread until the switch occurs).

3. Referring to claim 17 Joy has taught a computer based system for switching between program contexts comprising:

An embedded pipelined processor (Joy figure 3, column 8 lines 14-67) capable having a first program thread and a second program thread in an execution pipeline having a thread selection hardware (Joy figure 6, column 13 lines 5-23, column 15 lines 4-7);

A first set of data storage devices capable of storing a first thread state of said embedded processor (Joy figure 5 number 510 column 13 lines 5-23);

A second set of data storage devices capable of storing a second thread state of said embedded processor (Joy figure 5 number 512 column 13 lines 5-23); and

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A hardware thread scheduler for identifying which of said program threads said embedded processor executes (Joy figure 6 column 15 lines 4-7) and configurable to allocate available processing time of the embedded pipelined processor among at least the first and second states according to a fixed schedule (Joy figure 6, column 2 lines 40-45; the priority of

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the scheduler would be fixed, thus giving it a fixed schedule, since it would operate the same way each time it encounters the same threads);

Wherein said thread selection hardware in the embedded pipelined processor switches between said first and second thread state between consecutive instruction cycles in response to the hardware thread scheduler identifying of which of said program threads said embedded processor executes (Joy column 3 lines 45-56, column 6 lines 15-35 column 15 line 52-column 16 line 5; after the cycle ends, the second thread will now be in control for the next cycle).

4. Referring to claim 2 Joy has taught wherein said first state is the state of the embedded processor during the execution of the first program thread (Joy column 3 line 66-column 4 line 35).

5. Referring to claim 3 Joy has taught wherein said second state is the state of the embedded processor during the execution of the second program thread (Joy column 3 line 66-column 4 line 35).

6. Referring to claim 13 Joy has taught wherein said embedded processor is capable of restoring said second state of said embedded processor during execution of said first program thread (Joy column 3 lines 45-56, column 6 lines 15-35).

7. Referring to claim 14 Joy has taught wherein said embedded processor is capable of storing said second state of said embedded processor during execution of said first program thread (Joy column 3 lines 3-10; the information of state 2 will still be stored during the execution of state 1).

8. Referring to claim 15 Joy has taught wherein said first set of data storage devices comprises registers shared by a plurality of threads (Joy column 3 lines 3-10).

9. Referring to claim 16 Joy has taught wherein the fixed schedule is one of a fixed strict schedule, a semi-flexible strict schedule, and a loose strict schedule (Joy figure 6, column 2 lines 40-45; the priority of the scheduler would be fixed, thus giving it a fixed schedule, since it would operate the same way each time it encounters the same threads).

Referring to claim 19 Joy has taught a computer based method for switching between program contexts in an embedded multithreading pipelined processor (Joy figure 3, column 8 lines 14-67) having a hardware thread selector and an execution pipeline, the method comprising:

Storing a first context of said embedded processor in a first set of data storage devices, the first thread state corresponding to a first program thread (Joy figure 5 number 510 column 13 lines 5-23);

Storing a second context of said embedded processor in a second set of data storage devices, the second thread state corresponding to a second program thread (Joy figure 5 number 512 column 13 lines 5-23);

Switching the embedded processor from the first thread state to the second thread state (Joy figure 6 column 15 lines 4-7) between the end of the execution cycle and before the beginning of a next consecutive execution cycle by coupling the execution pipeline from the first set of data storage devices to the second set of storage devices via the thread selection hardware (Joy column 3 lines 45-56, column 6 lines 15-35 column 15 line 52-column 16 line 5; after the cycle ends, the second thread will now be in control for the next cycle).

10. Referring to claim 21 Joy has taught further comprising:

Identifying which of the said program threads said embedded processor executes according to an execution schedule (Joy figure 6 column 15 lines 4-7).

11. Referring to claim 22 Joy has taught further comprising allocating available processing time of the embedded pipelined processor among at least the first and second threads according to the execution schedule (Joy figure 6, column 2 lines 40-45).

12. Referring to claim 23 Joy has taught wherein the allocating comprises dividing the available execution time into a plurality of quanta, each quanta corresponding to a number of instruction cycles for execution of a thread (Joy figure 6, column 2 lines 40-45).

13. Referring to claim 24 Joy has taught wherein at least one quanta corresponds to a thread that is scheduled to execute periodically after a fixed number of execution cycles (Joy figure 6, column 2 lines 40-45).

### ***Claim Rejections - 35 USC § 103***

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

14. Claims 4 and 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Joy in

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view of Borkenhagen et al, U.S. Patent Number 6,567,839 (herein referred to as Borkenhagen).

15. Referring to claims 4 and 20 Joy has not taught wherein said processor switches between said first and second states by changing a state selection register.

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Borkenhagen has taught wherein said processor switches between said first and second states by changing a state selection register (Borkenhagen column 16 lines 38-49).

It would have been obvious to one of ordinary skill in the art at the time of the invention to use a register to change the threads of a multithreaded system. The system of Joy must have some mechanism to control the thread switch, but does not disclose details of this logic. Borkenhagen does disclose a particular embodiment for this logic and states reasoning to use this type of switching logic for such reason as assigning certain threads priority, which ties into the Joy system which has hard real time threads (Borkenhagen abstract, column 5 line 66-column 6 line 11). Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to look to Borkenhagen to use a register to change the threads of a multithreaded system if they want to do a detailed design since Joy does not describe that logic function.

16. Claims 5-9, 18, and 25-28 are rejected under 35 U.S.C. 103(a) as being unpatentable over Joy in view of Ramakrishnan et al, U.S. Patent Number 6,085,215 (herein referred to as Ramakrishnan).

17. Referring to claims 5, 25, and 26 Joy has not explicitly taught wherein said thread scheduler includes: A thread identifier for identifying at least one hard-real-time (HRT) thread and at least one non-real-time thread;

A HRT scheduler for regularly scheduling said HRT thread in available time quanta such that said HRT thread is scheduled to ensure the execution of the HRT in a predetermined time.

Ramakrishnan has taught wherein said thread scheduler includes:



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A thread identifier for identifying at least one hard-real-time (HRT) thread and at least one non-real-time thread (Ramakrishnan figures 2, 2a, and 2b, abstract, column 5 line 54-column 6 line 8, column 9 lines 9-21, column 15 line 39-column 16 line 6, column 8 lines 47-53);

A HRT scheduler for regularly scheduling said HRT thread in available time quanta such that said HRT thread is scheduled to ensure the execution of the HRT in a predetermined time (Ramakrishnan figures 2, 2a, and 2b, abstract, column 5 line 54-column 6 line 8, column 9 lines 9-21, column 15 line 39-column 16 line 6, column 8 lines 47-53).

It would have been obvious to one of ordinary skill in the art at the time of the invention to have a thread scheduler that handles real time threads so that real time threads will be executed when needed for critical systems needing real time operations. Ramakrishnan has taught this need for scheduling and has taught a solution with real time thread scheduling with general purpose threads and real time threads (Ramakrishnan column 1 lines 10-32, column 3 line 25-column 4 line 6, column 5 line 54-column 6 line 8). This will allow systems requiring real time operations to execute the required functions when needed, and the real time threads will have priority. Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to have a thread scheduler that handles real time threads to allow for real time threads to be completed when required.

18. Referring to claim 6 the combination of Joy and Ramakrishnan has taught wherein said time quanta is at least one instruction cycle (Ramakrishnan figures 2, 2a, and 2b, abstract, column 5 line 54-column 6 line 8, column 9 lines 9-21, column 15 line 39-column 16 line 6, column 8 lines 47-53; any switching would require some time, so it would take at least one unit of time, or one cycle).

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19. Referring to claim 18 the combination of Joy and Ramakrishnan has taught wherein said time quanta is exactly one instruction cycle (Ramakrishnan figures 2, 2a, and 2b, abstract, column 5 line 54-column 6 line 8, column 9 lines 9-21, column 15 line 39-column 16 line 6, column 8 lines 47-53; column 9 discusses how one time slot is used for the general purpose domain).

20. Referring to claims 7 and 27 the combination of Joy and Ramakrishnan has taught wherein said thread scheduler schedules a non-real-time (NRT) thread to replace a scheduled HRT thread if said HRT is complete (Ramakrishnan column 5 line 54-column 6 line 8, column 9 lines 9-21).

21. Referring to claim 8 the combination of Joy and Ramakrishnan has taught wherein said thread scheduler schedules the execution of non-real-time (NRT) threads in quanta not allocated to HRT threads (Ramakrishnan column 5 line 54-column 6 line 8, column 9 lines 9-21).

22. Referring to claims 9 and 28 the combination of Joy and Ramakrishnan wherein said thread scheduler regularly schedules NRT threads to be executed (Ramakrishnan column 5 line 54-column 6 line 8, column 9 lines 9-21).

23. Claims 10-12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Joy in view of Ramakrishnan in further view of Gutgold et al., U.S. Patent Number 6,026,503 (herein referred to as Gutgold).

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24. Referring to claim 10 the combination of Joy and Ramakrishnan has not taught wherein a first storage device for storing program instructions, said processor fetching instructions from the first storage device within a first fetch period;

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A second storage device for storing program instructions, said processor fetching instructions from the second storage device within a second fetch period;

Wherein said first fetch period is substantially shorter than said second fetch period.

Gutgold has taught wherein a first storage device for storing program instructions, said processor fetching instructions from the first storage device within a first fetch period;

A second storage device for storing program instructions, said processor fetching instructions from the second storage device within a second fetch period;

Wherein said first fetch period is substantially shorter than said second fetch period (Gutgold column 3 lines 1-19; it is well known in the art that flash memory is not as fast in operation as RAM memory, therefore having a slower fetch period than that of the RAM memory fetches).

It would have been obvious to one of ordinary skill in the art at the time of the invention to use two different memories to fetch instructions from. Gutgold has taught storing the debug executable information in the EEPROM, or ROM, and that having a debug mode for a processor is beneficial since it allows the user to test the code they have written just as programmers test code on an emulator (Gutgold column 1 lines 27-45 and column 2 lines 20-26). By being able to test the code, the user can make sure the code runs efficiently and correctly. Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to be able to debug the program code just as an emulator would, allows the program to be tested to make sure that is correct and does not causes errors.

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25. Referring to claim 11 the combination of Joy and Ramakrishnan and Gutgold has taught wherein said first storage device for storing program instructions comprises a static RAM (Gutgold column 3 lines 1-19).

26. Referring to claim 12 the combination of Joy and Ramakrishnan and Gutgold has taught wherein said second storage device for storing program instructions comprises a flash memory (Gutgold column 3 lines 1-19).

### ***Response to Arguments***

27. Applicant's arguments filed 7/22/04 with respect to claims have been considered but are moot in view of the new ground(s) of rejection.

### ***Conclusion***

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Charles A Harkness whose telephone number is 703-305-7579. The examiner can normally be reached on 8Flex.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on 703-305-9712. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

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Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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Charles Allen Harkness

Patent Examiner

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October 14, 2004



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